PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H03M 13/22, G06F 12/06, 12/02

A1

(11) International Publication Number: WO 96/37050

(43) International Publication Date: 21 November 1996 (21.11.96)

(21) International Application Number: PCT/US96/04758

(22) International Filing Date: 4 April 1996 (04.04.96)

(30) Priority Data:
08/441,078 15 May 1995 (15.05.95) US

(71) Applicant: ADVANCED HARDWARE ARCHITECTURES, INC. [US/US]; 2365 N.E. Hopkins Court, Pullman, WA 99163-5601 (US).

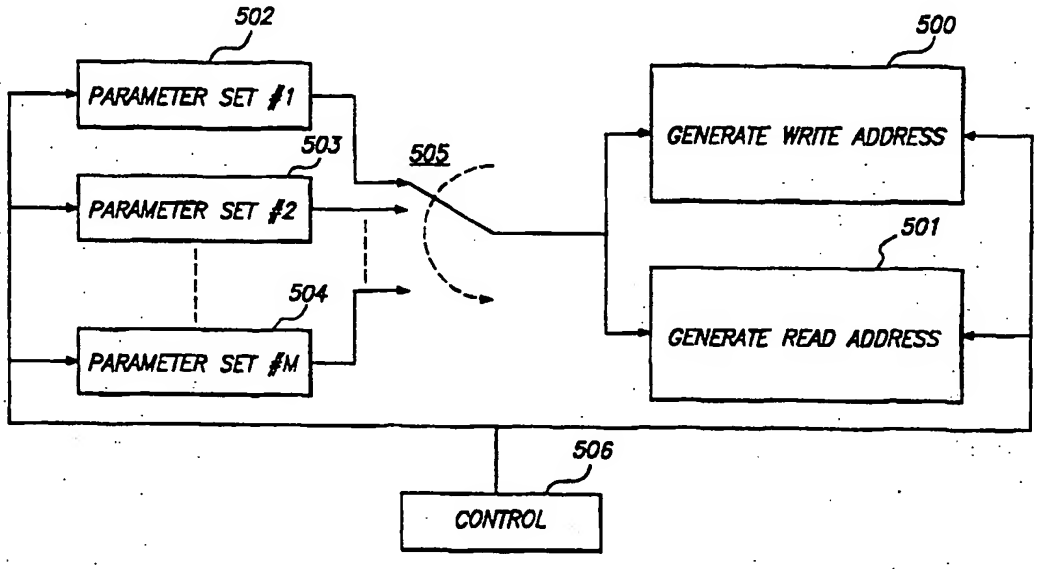
(72) Inventors: ZWEIGLE, Greg; N.W. 1552 Leland, Pullman, WA 99163 (US). BERGE, Torkjell; 624 Sherwood Street, Moscow, ID 83843 (US).

(74) Agents: HAVERSTOCK, Thomas, B. et al.; Haverstock & Associates, Suite 420, 260 Sheridan Avenue, San Francisco, CA 94306 (US).

(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: RECONFIGURABLE INTERLEAVER/DEINTERLEAVER AND ADDRESS GENERATOR FOR DATA STREAMS INTERLEAVED ACCORDING TO ONE OF A PLURALITY OF INTERLEAVING SCHEMES



(57) Abstract

A cost effective deinterleaving apparatus is selectively configurable for data streams interleaved according to one of a plurality of interleaving schemes. This is accomplished by providing a plurality of parameter sets for the apparatus with each set corresponding to a particular deinterleaving algorithm. A user is then able to selectively choose a particular deinterleaving algorithm with which to apply an input interleaved scheme. The low cost is achieved by reusing a single apparatus for all deinterleaving algorithms and changing only a few key parameters. Examples of applicable deinterleaving algorithms include Ramsey and Forney. Since any deinterleaver is also an interleaver, this invention is useful for interleaving as well.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgystan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic			SE	Sweden
CG	Congo	KR	Republic of Korea	SG	Singapore
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LR	Liberia	SZ	Swaziland
CS	Czechoslovakia	LT	Lithuania	TD	Chad
CZ	Czech Republic	LU	Luxembourg	TG	Togo
DE	Germany	LV	Latvia	TJ	Tajikistan
DK	Denmark	MC	Monaco	TT	Trinidad and Tobago
EE	Estonia	MD	Republic of Moldova	UA	Ukraine
ES	Spain	MG	Madagascar	UG	Uganda
FI	Finland	ML	Mali	US	United States of America
FR	France	MN	Mongolia	UZ	Uzbekistan
GA	Gabon	MR	Mauritania	VN	Viet Nam

BNSDOCID: <WO___9637050A1_I_>

RECONFIGURABLE INTERLEAVER/DEINTERLEAVER AND ADDRESS GENERATOR FOR DATA STREAMS INTERLEAVED ACCORDING TO ONE OF A PLURALITY OF INTERLEAVING SCHEMES.

FIELD OF THE INVENTION

The invention relates to the field of data processing and can be used to aid communication systems which require noise tolerance.

BACKGROUND OF THE INVENTION

Communication systems use interleavers to transform data which has been corrupted by correlated noise into data in which the noise appears to be distributed in time with less correlation. The deinterleaver transforms the data back into its original form. The overall interleave/deinterleave operation is such that the received data is identical to the transmitted data in the absence of noise. Several algorithms have been developed which perform the interleave/deinterleave function. These algorithms lend themselves to different implementations, each with their own advantages and disadvantages.

Two well known algorithms for interleaving and deinterleaving data were developed by John Ramsey and David Forney. John Ramsey's original work contains four different interleavers called type I, type II, type III, and type IV.

Figure 1 illustrates Ramsey's original implementation of his type II interleaver. There are two parameters for the interleave, n2 and n1. The n2 parameter specifies how many contiguous symbols in the interleaved sequence over which the minimum spacing n1 is valid. The n1 parameter specifies the minimum spacing in the original stream that can be contained in any n2 contiguous symbols in the interleaved stream. In Fig. 1 the blocks 101, 102, 103, and 104 are shift registers with delay n2-1. The blocks 106, 107, 108, and 109 are adders which serve as muxes when n1 and n2 are constrained appropriately. The constraints on n2 and n1 are that n2 and n1+1 must be relatively prime and $n2 > n1+1$. The commutator switch 105 sequences counter-clockwise for every symbol received at

the input 111. The continuation symbol 110 indicates that the number of shift and add stages is not explicitly specified by the drawing. For this implementation, a total of n1*(n2-1) delay elements are required. The output is from 112.

Figure 2 illustrates a basic Forney type interleaver. The shift registers 200, 201, 202, and 203 are of length specified inside the register and shift the data one position to the right every I^{th} input data symbol. For example, the shift register 200 has a total delay of T*I and the shift register 201 has a total delay of 2*T*I. There are a total of I sets of shift registers. The commutators 204 and 205 move one position every input symbol and are synchronized with each other. In this document the value T*I is defined as N. There are a total of I*(I-1)*T/2 delay elements for the interleaver. A forney interleaver is equivalent to ta Ramsey type III (not shown here) when N = n1+1 and I = n2 and T is an integer.

In the state of the art, there are two basic approaches to implementing the algorithms invented by Forney and Ramsey. One approach is with the use of shift registers and this was the technique presented in the inventor's original works. This technique has the advantage of requiring the smallest number of memory elements. Another approach is with the use of a random access memory (RAM). This technique has the advantage of using a cheaper technology. A diagram contrasting these approaches is shown in Figure 3. In Fig. 3a, the data arrives as 306 and exits either interleaved or deinterleaved as 307. The shift register is 304 and the commutators 308 and 309. The control is shown as 305. In Fig. 3b, the RAM is 300. Data is written into the RAM in 302 and is read from the RAM is 303. The 301 is the address generation and control for the operation.

An apparatus implementing a single deinterleaving algorithm (such as those designed to deinterleave streams interleaved according to the techniques described above) suffers from the drawback of only being able to deinterleave data streams interleaved by a single protocol. This proves particularly troublesome when users wish to design a system that can receive and deinterleave data interleaved using different interleaving algorithms. In the United States, the standard interleaving protocol for Direct Broadcast Satellite (DBS) systems is based on Ramsey's type II algorithm. In Europe, the protocol for DBS systems is based on Forney's algorithm. The result is that users must use a different deinterleaving apparatus

than when they deinterleave DBS data streams initiated in the United States as opposed to data streams from Europe. Similarly, manufacturers of deinterleaving equipment must build different devices for sale in the United States and Europe.

What is needed is an apparatus that can be reconfigured to deinterleave streams interleaved according to a plurality of interleaving schemes.

SUMMARY OF THE INVENTION

The present invention provides a cost effective deinterleaving apparatus that is selectively configurable for data streams interleaved according to one of a plurality of data streams (note that since a deinterleaver is also an interleaver this invention also is a configurable interleaving apparatus). This is accomplished with the invention of a single, cost efficient address generation unit that can be used for multiple algorithms by dynamically controlling key parameters during operation. The system level diagram of the deinterleaver is similar to that shown in Fig. 3b and Fig. 4. The key distinction is that the address generation and control unit is capable of deinterleaving a plurality of interleaved data streams with a cost efficient technique. It should be noted that there are no special constraints placed on the RAM by this invention. It can be any standard type, such as dynamic or static, single port or multiple port.

According to the preferred embodiment of the present invention a Generate Write Address block remains the same for all interleaving protocols. It generates an address for writes which restarts every time the last address is written. A Generate Read Address block also remains the same for all interleaving protocols. It generates the read address for a RAM. The parameters specific to each interleaving algorithm are generated in a Parameter Set block. There can be an arbitrary number of Parameter Set blocks, one for each interleaving protocol. A switch selects the correct set of parameters for each interleaving protocol. Such a device allows the deinterleaving apparatus to receive a data stream which has been interleaved according to one of a plurality of interleaving schemes and output the original data stream. A control block is the same for all interleaved data streams and allows the address generation and parameter units to update based on data either being written to or read from the RAM. The Generate Write Address,

Generate Read Address and control blocks are used for all interleaving protocols, thereby providing cost efficiency. Additionally, in the preferred embodiment, the most complexity in these three blocks. This allows the Parameter Set blocks to be produced at very low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a Ramsey type II interleaver as described by John L. Ramsey.

Figure 2 illustrates a Forney interleaver similar to description of David G. Forney.

Figure 3 illustrates two different implementations of interleaver/deinterleavers in the state of the art.

Figure 4 illustrates a block diagram of one embodiment of a circuit which performs deinterleaving according to a plurality of protocols.

Figure 5 illustrates the a block diagram of the preferred embodiment of the present invention.

Figure 6 illustrates one example of a hardware implementation of the address generation unit for deinterleaving a Ramsey type II or Forney interleaved data stream.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is for a deinterleaving apparatus that would be reconfigurable by a user to deinterleave a data stream according to the Ramsey type II or the Forney protocols, or even using a proprietary scheme. This will provide users with a deinterleaver that has greater applicability. More specifically, it allows a user in the United States to receive and deinterleave interleaved data from Europe without having to purchase a deinterleaving apparatus utilizing a different algorithm.

One technique for providing a multipurpose deinterleaver is to include the appropriate circuitry for all desired deinterleavers in a single apparatus and then use a hardware or software switch to engage the desired deinterleaver. Such a system for deinterleaving one of two types of interleaved data is shown in Figure 4 for the

RAM based deinterleave implementation approach. In Fig. 4, the RAM is 400, the data is in 403, and the data out is 404. The two different address generation units and control are shown as 401 and 402. The switch 405 is used to activate the desired deinterleaving algorithm. This "brute-force" scheme has the disadvantage of requiring a completely separate apparatus for each allowable type of interleaved data. For software implementation, requiring multiple separate apparatuses requires multiple sizes of the program memory. For hardware implementation on an integrated circuit, the multiple separate apparatuses require more transistors and therefore more silicon area. In the design of integrated circuits, silicon area is a critical parameter in manufacturing cost and therefore must be minimized wherever possible. Furthermore, the high cost of having a separate apparatus for each deinterleaving protocol gets worse as more protocols are added to the deinterleaver.

Figure 5 shows a block diagram of the preferred embodiment of the present invention which is used in place of 301 in Fig. 3 or in place of 401, 402, and 405 in Fig. 4. The Generate Write Address block 500 remains the same for all interleaving protocols. It generates an address for writes which restarts every time the last address is written. The Generate Read Address block 501 remains the same for all interleaving protocols. It generates the read address for the RAM. The parameters specific to each interleaving algorithm are generated in the Parameter Set blocks 502, 503, and 504. There can be an arbitrary number of these units, one for each interleaving protocol. The commutator 505 switches the correct set of parameters into 500 and 501 for each interleaving protocol. When this device is used in place of 301 in Fig. 3, it allows apparatus 300 to receive a data stream 302 which has been interleaved according to one of a plurality of interleaving schemes and output the original data stream to 303. The control block 506 is the same for all interleaved data streams and allows the address generation and parameter units to update based on data either being written to the RAM through 302 or read from the RAM through 303. Because the blocks 500, 501, and 506 are reused for all interleaving protocols, cost efficiency is achieved. Furthermore, this invention places the most complexity in blocks 500, 501, and 506 and therefore the parameter sets 502, 503, and 504 can be very low cost.

Figure 6 shows one possible hardware implementation of the invention of Figure 5. This example deinterleaves two possible types of interleaved data streams, the Ramsey type II interleaved data stream and the Forney interleaved data stream. This example is designed to work with a single port RAM which requires reads and writes to be disjoint in time, hence the mux 605. For this implementation a read always precedes a write since the same address can generated by both the read address 604 and write address 600 circuitry. Another possible hardware implementation for a dual port RAM allows concurrent reads and writes and would eliminate the need for the mux 605.

Blocks 605, 606, 607, 608, 609, 610, and all objects labeled 612 are two input muxes. These devices route either the '0' input or the '1' input to the 'm' output based on the value of the select signal arriving at the side of the object. All blocks labeled 611 are summation devices and the block labeled 613 is a subtraction device. All blocks labeled 614 are data storage devices. All blocks labeled 615 are equality comparators, whose output goes active when the equality test is evaluated true. The block 616 is a greater-than-or-equal-to comparator.

The Write Address Generation Unit 600 increments linearly through the RAM address space until it reaches the RAM size, selected by the mux 606, at which time it starts over at the first address. The go_write signal tells the write address to increment every time a byte is received at the RAM and is generated by the control 506 (Figure 5).

The Read Address Generation Unit 604 changes the read address when the go_read signal is asserted indicating that data is to be removed from the RAM. The go-read signal is generated by the control 506 and will not begin to assert until the RAM has been completely written once. After this time, the go_read signal always asserts when a new byte is received at the RAM. In other words, once the RAM has been written once, data is read out of the RAM only when data is written into the RAM. To flush the RAM, a dummy byte can be written under control 506. When the read address exceeds the RAM size, muxed through 606, then the RAM size is subtracted from the read address.

The two sets of parameters 601 and 602 are shown in the example of Figure 6. The Ramsey II parameter set 601 provides dynamic information to the Read

Address Generation Unit 604. The Forney parameter set 602 provides fixed information to the Read Address Generation Unit 604. The set of muxes 603 perform the function of the commutator 505 (Figure 5) and is set before deinterleaving occurs. In the set of muxes for this implementation are the RAM size, from mux 606; an additional count number of 0 or 1, from mux 607 the Ramsey type II n1 parameter, from mux 608; a count parameter, from mux 609; and a mux select signal from mux 610. The select signal to mux group 603 chooses among the two interleave types.

The Ramsey type II deinterleave is performed by noticing from Figure 1 that the original data is ordered by offsets of n2 except every n1+1 it is offset by n2+n1+1. The circuit pair 601 and 604 generate the read addresses to extract the original ordering out of the interleaved data stream.

The Forney deinterleave performs by noticing from Figure 2 that Forney interleaved data has the original data ordered by offsets of N+1. Deinterleaving is accomplished by reading in steps of N+1 until N*1 is reached at which time the read address N*I-(N+1)*I = I is read which is the I^{th} data of the original stream. Then steps of N+1 continue. The circuit pair 602 and 604 generate the read addresses to extract the data out of the interleaved data stream.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to one of ordinary skill in the art that the apparatus disclosed above is only illustrative of the preferred embodiment of the present invention and is in no way a limitation.

CLAIMS

We claim:

1. A deinterleaving apparatus comprising a data input for receiving a stream of data that was interleaved according to one of a plurality of interleaving algorithms, and a control input for receiving a signal for selectively configuring the apparatus to deinterleave the stream of interleaved data according to a predetermined deinterleaving algorithm.

2. The deinterleaving apparatus according to claim 1 further comprising an interleaving circuit coupled to the data input for selectively configuring the apparatus to interleave a stream of data.

3. An interleaving/deinterleaving apparatus, comprising:

a. an input means for receiving an input stream of data bytes;

b. a random access memory having a plurality of data byte storage locations coupled to receive the input stream;

c. a write address generator coupled to the memory for directing each byte in the input stream to an appropriate one of the storage locations;

d. a read address generator coupled to the memory for selecting which of the locations will provide a data byte to an output stream;

e. an output means coupled to the memory for receiving the output stream; and

f. a controller coupled to the memory, the write address generator and the read address generator, the controller including a plurality of parameter sets, each parameter set for allowing the controller to interleave or deinterleave an input stream according to one of a plurality of interleaving algorithms.

4. The interleaving/deinterleaving apparatus according to claim 3, wherein the write address generator and controller place an input stream into the memory, by linearly incrementing a storage location address from a first address to a last address and wherein the read address generator selects locations according to a selected on of the interleaving algorithms.

5. The interleaving/deinterleaving apparatus according to claim 3, wherein one of the parameter sets directs the controller to execute a Ramsey II interleaving algorithm.

6. The interleaving/deinterleaving apparatus according to claim 3, wherein one of the parameter sets directs the controller to execute a Forney interleaving algorithm.

7. A de-interleaving apparatus selectively configurable for data streams interleaved according to one of a plurality of interleaving schemes, the de-interleaving apparatus comprising:

a. an input means for receiving a data stream interleaved according to one of a plurality of interleaving schemes;

b. a plurality of de-interleaving means coupled to the input means for de-interleaving the data stream according to a specific de-interleaving algorithm;

c. a switch means coupled between the input means and the plurality of de-interleaving means for allowing a user to selectively route the data stream through a specific de-interleaving means; and

d. an output means coupled to the de-interleaving means for outputting a de-interleaved data stream representing the original data.

8. The de-interleaving apparatus according to claim 7 wherein each of the plurality of de-interleaving means further comprises:

a. a read enable means for reading a byte from the data stream interleaved according to one of a plurality of interleaving schemes;

b. a write enable means coupled to the read enable means for writing a byte of the interleaved data stream; and

c. a random access memory coupled to the write enable means for storing a reordered sequence of data corresponding to an original data stream.

9. The de-interleaving apparatus according to claim 7 wherein the plurality of de-interleaving means includes a de-interleaver configured to de-interleave a data stream interleaved according to a Ramsey II interleaving scheme.

10. The de-interleaving apparatus according to claim 7 wherein the plurality of de-interleaving means includes a de-interleaver configured to de-interleave a data stream interleaved according to a Ramsey III interleaving scheme.

11. A method of de-interleaving a data stream interleaved according to one of a plurality of interleaving schemes comprising the steps of:

a. inputting a stream of interleaved data;

b. routing the stream of data through a user selected one of a plurality of data paths each path corresponding to a different de-interleaving algorithm;

c. de-interleaving the stream of data within one of the configured data paths to form an original stream of data; and

d. outputting an original stream of data.

12. The method of de-interleaving a data stream according to claim 11 wherein the step of de-interleaving further comprises the steps of:

a. reading a byte of data from the stream of interleaved data; and

b. writing the byte of data to a specific random access memory location according to a de-interleaving algorithm corresponding to the user selected data path.

13. The method of de-interleaving a data stream according to claim 11 wherein the step of routing the stream of data includes routing the stream of data through a data path corresponding to a Ramsey II de-interleaving algorithm.

14. . The method of de-interleaving a data stream according to claim 11 wherein the step of routing the stream of data includes routing the stream of data through a data path corresponding to a Ramsey III de-interleaving algorithm..

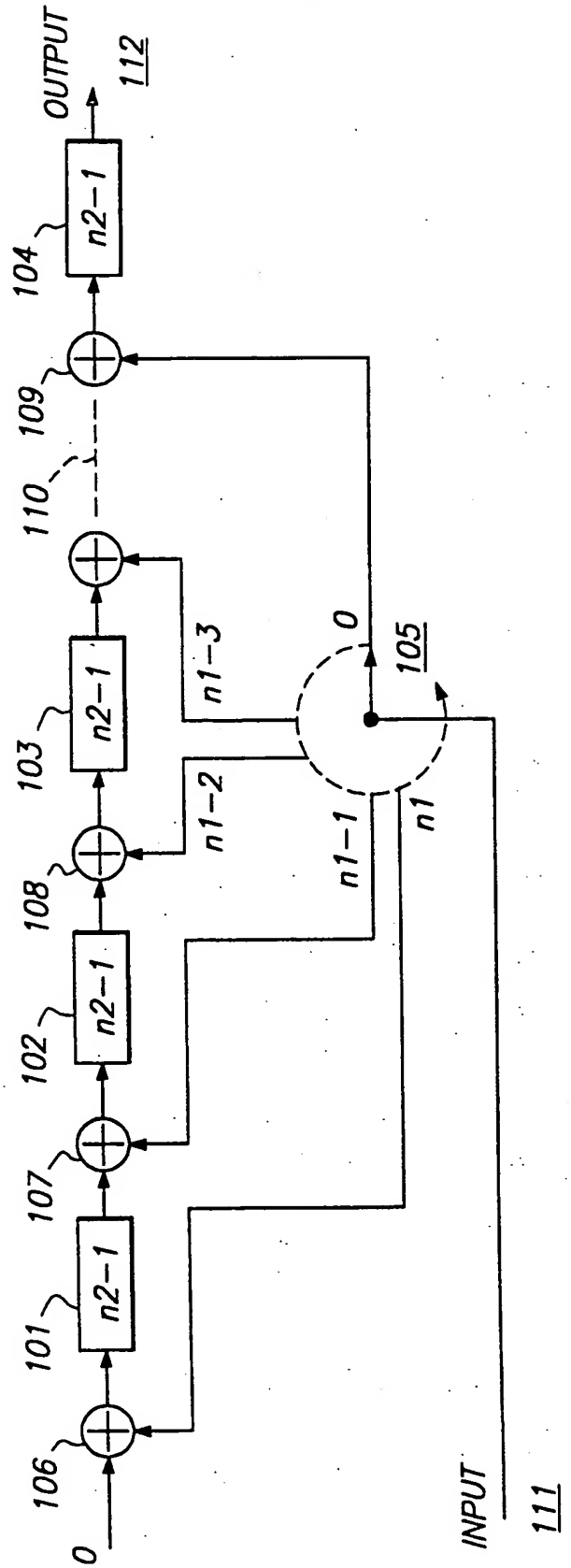

OUTPUT
112
104
n2-1
109
110
103
n2-1
n1-3
0
105
108
n1-2
n1-1
n1
102
n2-1
107
101
n2-1
106
0
INPUT
111

FIG. 1

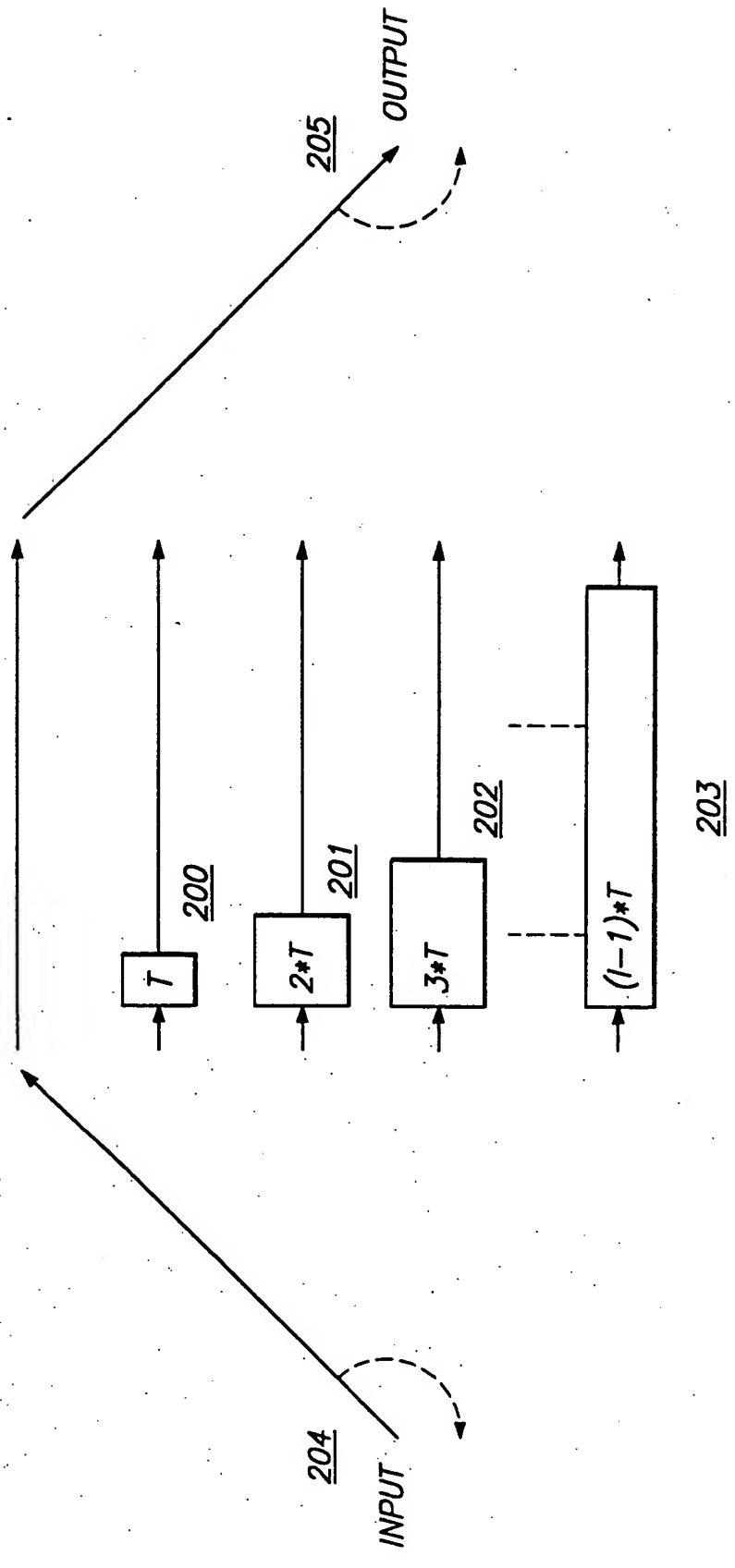


FIG. 2

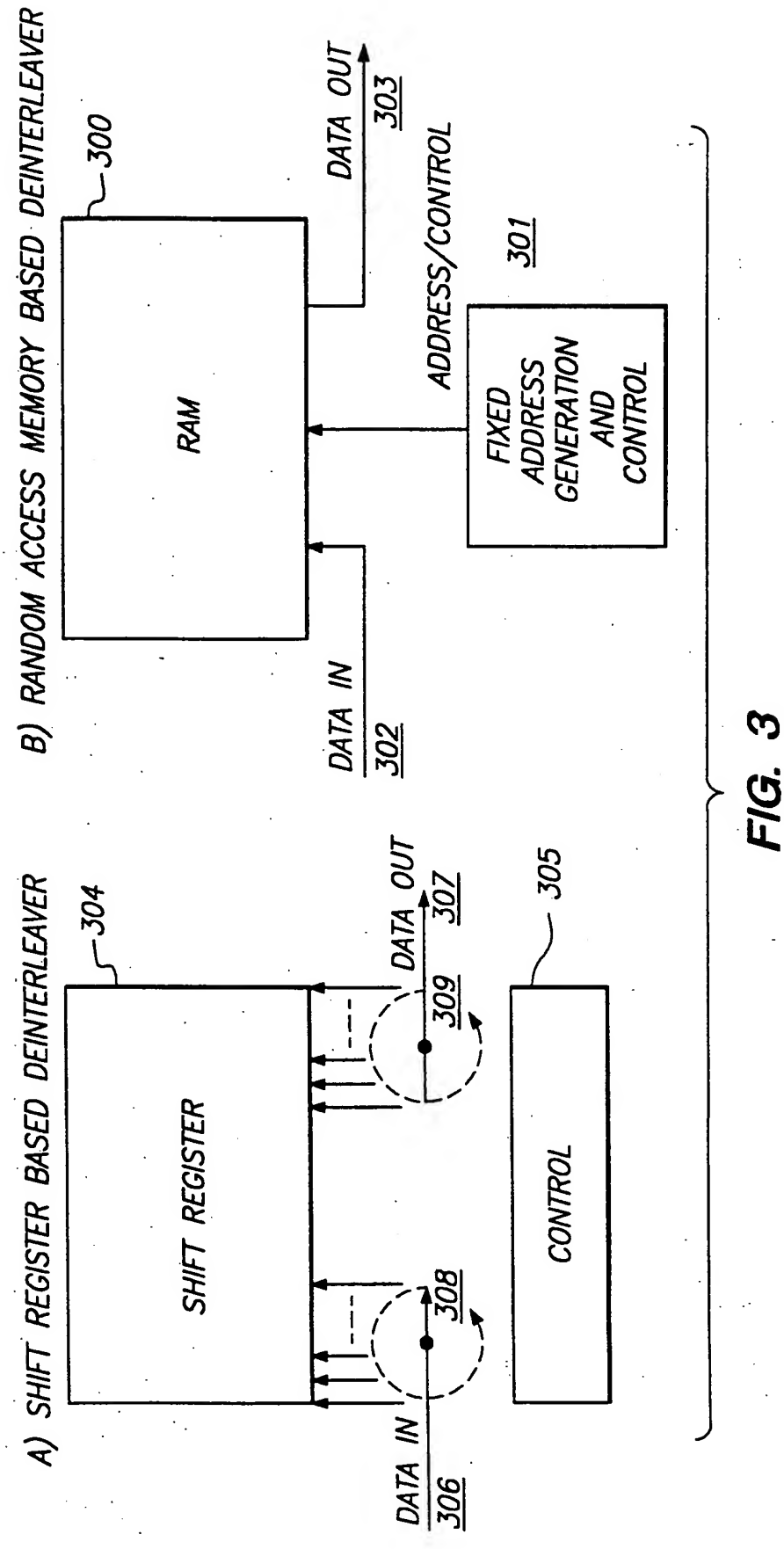


FIG. 3

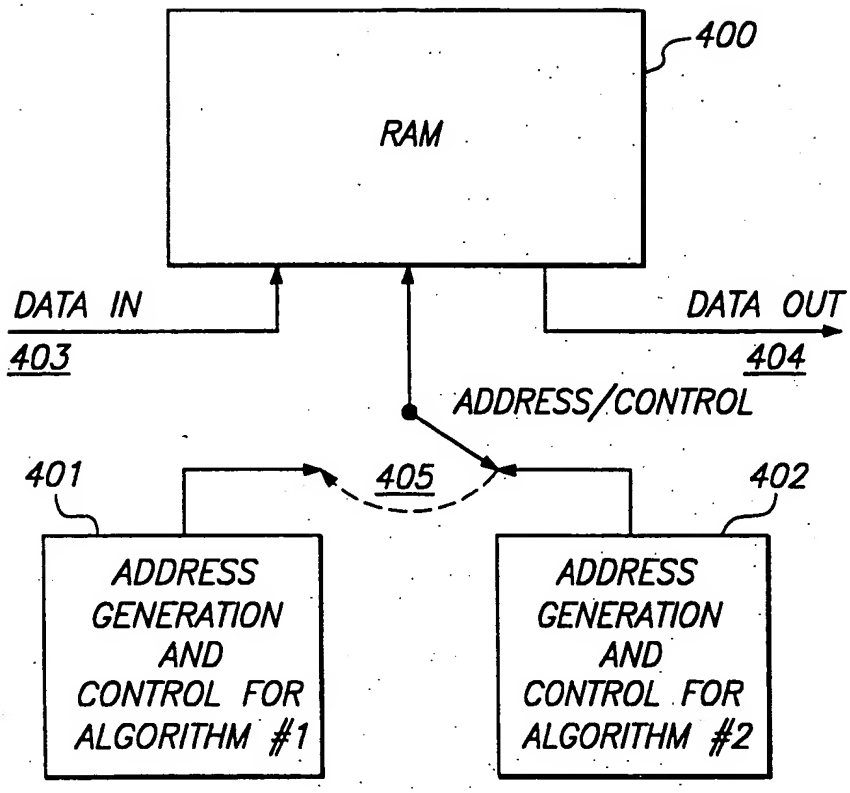


FIG. 4

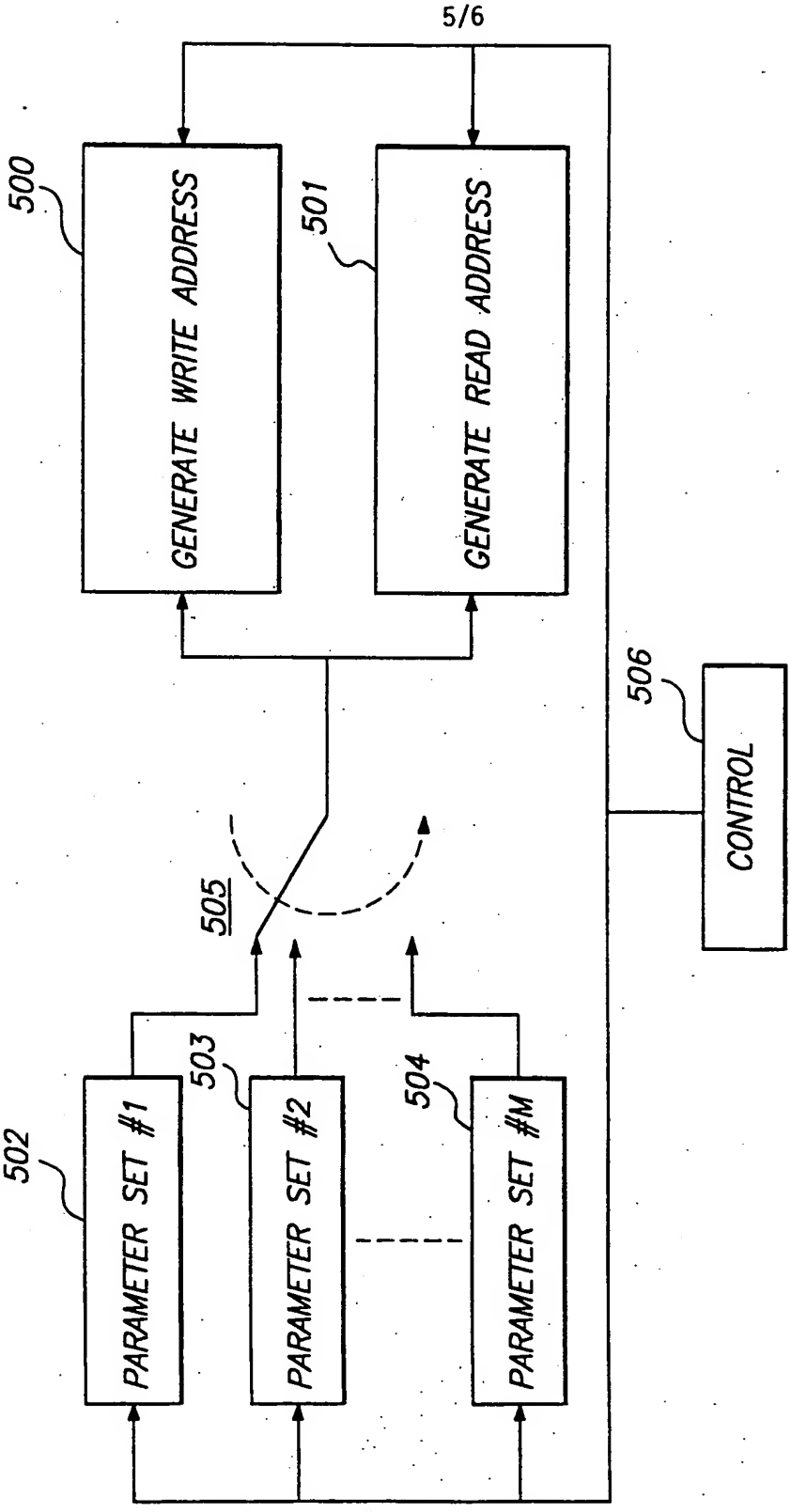

500
GENERATE WRITE ADDRESS
501
GENERATE READ ADDRESS
506
CONTROL
505
502
PARAMETER SET #1
503
PARAMETER SET #2
504
PARAMETER SET #M

FIG. 5

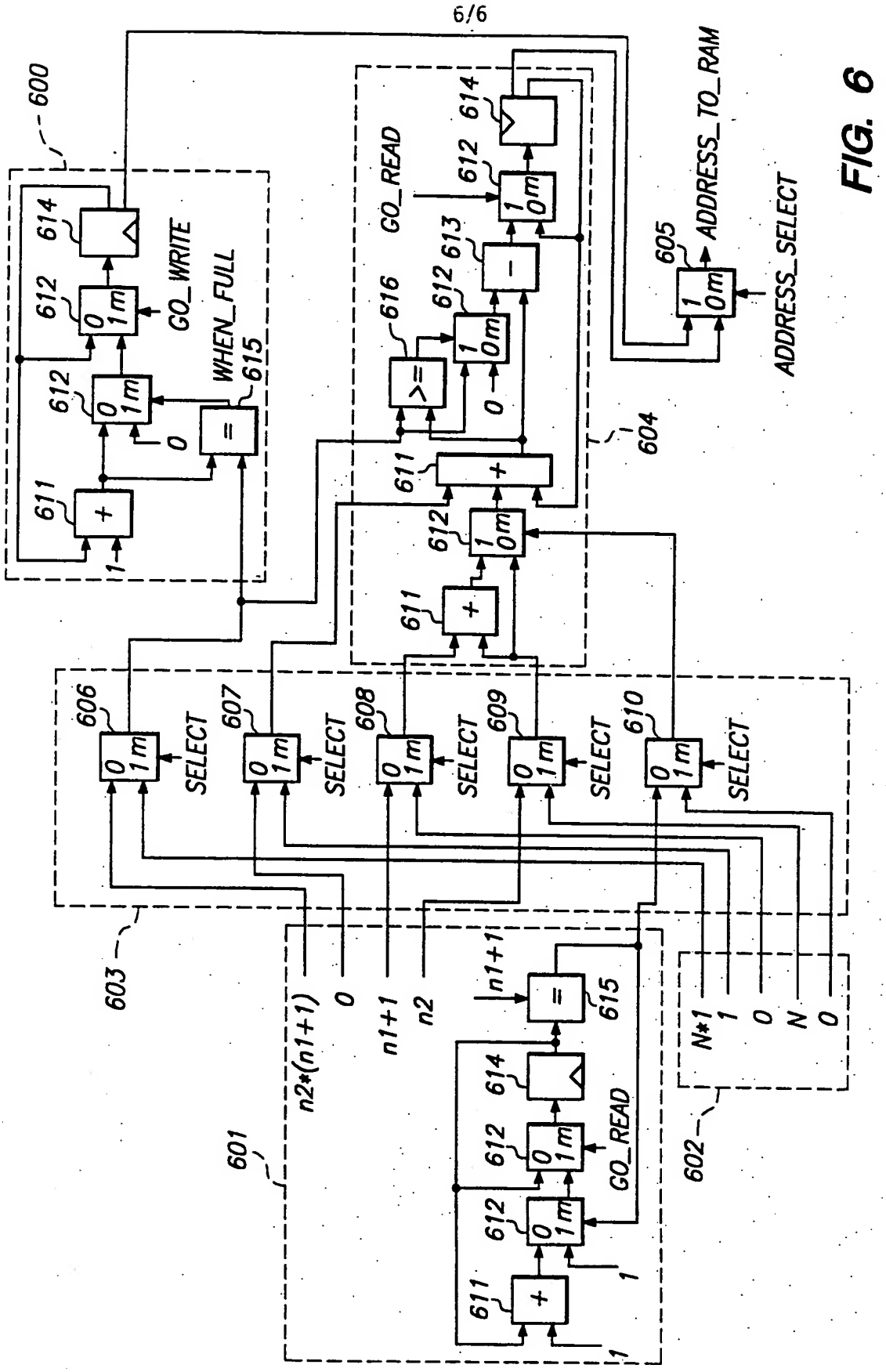

600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
GO_WRITE
WHEN_FULL
GO_READ
ADDRESS_TO_RAM
ADDRESS_SELECT
SELECT
n2*(n1+1)
n1+1
n2
N*1

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/04758

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M13/22 G06F12/06 G06F12/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 901 319 (ROSS) 13 February 1990 see abstract see column 1, line 45 - line 68 see column 3, line 39 - column 5, line 10 see claims; figures ---	1-14
Y	EP,A,0 569 716 (SONY CORPORATION) 18 November 1993 see abstract see column 2, line 53 - column 3, line 18 see column 7, line 37 - line 52 ---	1-14
Y	US,A,5 063 533 (ERHART ET AL.) 5 November 1991 see the whole document --- -/--	1-14

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 August 1996	13. 09. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Gries, T

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 042 033 (COSTA) 20 August 1991 see abstract see figures see column 2, line 17 - column 3, line 14 see claims; figures	1-14
A	US,A,5 136 588 (ISHIJIMA) 4 August 1992 see column 2, line 13 - column 3, line 27	1-14
A	BRIDGING THE GAP BETWEEN INTEROPERABILITY, SURVIVABILITY, SECURITY, BOSTON, OCT. 15 - 18, 1989 THREE VOLUMES BOUND AS ONE, vol. 1 OF 3, 15 October 1989, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 6-10, XP000130705 DARMON M M ET AL: "A NEW PSEUDO-RANDOM INTERLEAVING FOR ANTIJAMMING APPLICATIONS" see page 6, right-hand column, paragraph 5 - paragraph 7 see page 7, line 1 - page 10, paragraph 3	1-14
A	IEEE TRANSACTIONS ON INFORMATION THEORY, MAY 1970, USA, vol. IT-16, no. 3, ISSN 0018-9448, pages 338-345, XP002010849 RAMSEY J L: "Realization of optimum interleavers" see the whole document	5,9,10, 13,14
A	IEEE TRANSACTIONS ON COMMUNICATION TECHNOLOGY, OCT. 1971, USA, vol. COM-19, no. 5, suppl., ISSN 0018-9332, pages 772-781, XP002010848 FORNEY G D JR: "Burst-correcting codes for the classic bursty channel" see page 775, right-hand column, paragraph 2 - page 777, right-hand column, paragraph 1; figures 2-6	6
A	EP,A,0 552 979 (SAMSUNG ELECTRONICS CO.) 28 July 1993 see abstract; claims; figures	1-14
A	EP,A,0 282 070 (FUJITSU LTD.) 14 September 1988 see abstract; figures; tables	1-14
A	US,A,4 394 642 (CURRIE ET AL.) 19 July 1983 see abstract; claims; figures	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/04758

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4901319	13-02-90	NONE		
EP-A-569716	18-11-93	JP-A-	5290527	05-11-93
		US-A-	5528608	18-06-96
US-A-5063533	05-11-91	NONE		
US-A-5042033	20-08-91	NONE		
US-A-5136588	04-08-92	JP-A-	1037125	07-02-89
		WO-A-	8901265	09-02-89
EP-A-552979	28-07-93	NONE		
EP-A-282070	14-09-88	JP-A-	63225837	20-09-88
		AU-B-	599762	26-07-90
		CA-A-	1295423	04-02-92
		DE-D-	3850896	08-09-94
		DE-T-	3850896	22-12-94
		US-A-	5134695	28-07-92
US-A-4394642	19-07-83	NONE		